A Non-Linear Analysis of the Saturated MOSFET

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The maximum power and the maximum efficiency at the maximum power have been derived for the MOSFET when the MOSFET is in saturation over the entire cycle, using the square law theory. Results are presented for the following three cases: the gate voltage is a sinusoid, a half sinusoid and a square wave. Results using the square law theory and bulk-charge theory for analysis of the MOSFET are compared.

When a MOSFET is saturated, the drain current is not a function of the drain voltage; it is only a function of the gate voltage. The load impedance thus has no effect on the drain current. The MOSFET amplifier can therefore be easily analyzed if the MOSFET is in saturation over the complete cycle. In this paper, the n-type MOSFET amplifier is analyzed utilizing the non-linear equations that describe the physics of the MOSFET, for the case where the MOSFET is in saturation for the entire cycle. A similar analysis is given in [1] for the JFET. For a given input excitation, the drain current can be calculated as a function of time and the Fourier components can be calculated. The output power and the efficiency can then be calculated for a given load resistance and DC bias voltage. For the n-type MOSFET, the maximum power and the maximum efficiency at the maximum power are presented for a given load resistance when the gate voltage is a sinusoid, a half sinusoid and a square wave. The maximum power and efficiency are compared for these three excitations.

The MOSFET: Sinusoidal Input Voltage Excitation—Square Law Theory

There are two theories for obtaining a relationship for the drain current as a function of the gate voltage, when the MOSFET is in saturation; the square law theory and the bulk-charge theory. In the following analysis the square law theory will be used as it is simpler and gives good insight into the performance of the MOSFET. The results will then be compared to the results using the bulk-charge theory. I_{dsat} is given by Eq. 1 when using the square law theory [2].

$$I_{dsat} = (Z\mu'_n C_0/2L)(V_g - VT)^2 \quad (1)$$

where I_{dsat} is the drain current when the MOSFET is in saturation, μ'_n is the average mobility of the inversion layer carriers, C_0 is the oxide capacitance, Z is the width of the channel and L is its length.

The first case considered is the sinusoidal case where V_g is given by Eq. 2.

$$V_g = (V_{gmax} + V_T)/2 + [(V_{gmax} - V_T)/2] \cos(\omega t) \quad (2)$$

V_g has a maximum value of V_{gmax} and a minimum value of V_T. Substituting Eq. 2 into Eq. 1 yields:

$$I_{dsat} = (Z\mu'_n C_0/2L)[(V_{gmax} - V_T)(1 + \cos(\omega t))/2]^2 \quad (3)$$

I_{dss}, the maximum saturated drain current, is given by Eq. 1 with V_g set equal to V_{gmax}.

$$I_{dss} = (Z\mu'_n C_0/2L)(V_{gmax} - V_T)^2 \quad (4)$$

Dividing Eq. 3 by Eq. 4 yields Eq. 5.

$$I_{dsat}/I_{dss} = [(1 + \cos(\omega t))/2]^2$$

$$= 3/8 + 1/2 \cos(\omega t) + 1/8 \cos(2\omega t) \quad (5)$$

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Eq. 5 yields a DC current I_0I_{dss}, equal to $(3/8)I_{dss}$ and a current at the fundamental frequency I_1I_{dss} equal to $I_{dss}/2$. The DC power is given by Eq. 6.

$$P_0 = I_0I_{dss}V_0 = (3/8)I_{dss}V_0 \quad (6)$$

where V_0 is the DC bias voltage. The output power at the fundamental frequency P_1, is given by Eq. 7.

$$P_1 = (I_{dss}I_1)^2R_L/2 \quad (7)$$

The drain current is not a function of the drain voltage when the MOSFET is in saturation; it is only a function of the gate voltage and it therefore is not affected by the load impedance. Since only the fundamental frequency is desired at the output, the load impedance should present a short-circuit at all of the harmonic frequencies. Only voltage at the fundamental frequency will then appear across the drain and across the load resistor. Since for a MOSFET, V_{dsat} is equal to $(V_g - V_T)$ [2], the constraint that the MOSFET is in saturation over the entire cycle and the harmonics are short circuited to ground requires that the amplitude of the fundamental frequency can be no greater than $V_0 - (V_{gmax} - V_T)$. The minimum value of the drain voltage is then equal to $(V_{gmax}-V_T)$, which is the saturation voltage when the gate voltage is equal to V_{gmax} and the maximum value is equal to $2V_0 - (V_{gmax} -V_T)$. Since the drain current flowing through the load resistor is sinusoidal and has a value I_1I_{dss},the load resistance is given by Eq. 8.

$$R_L = (V_0 - (V_{gmax} - V_T)|) /(I_1I_{dss}) \quad (8)$$

Solving Eq. 8 for V_0 yields Eq. 9.

$$V_0 = (I_1I_{dss})\, R_L + (V_{gmax} - V_T) \quad (9)$$

Substituting Eq. 8 into Eq. 7 yields the output power at fundamental-frequency, P_1, given by Eq. 10:

$$P_1 = (I_1I_{dss})^2R_L/2 = (I_1I_{dss})\,(V_0 - (V_{gmax} - V_T))/2 \quad (10)$$

The output power for the sinusoidal case is thus given by Eq. 11.

$$P_1 = .25(\, I_{dss})\,(V_0 - (V_{gmax} - V_T)) \quad (11)$$

The efficiency is given by Eq. 12:

$$Eff = P_1 /P_0 = EFF0(V_0 - (V_{gmax} - V_T))/V_0 = (I_1 /2I_0)(V_0 - (V_{gmax} - V_T))/V_0 \quad (12)$$

where EFF0 is equal to $I_1/2I_0$, which is equal to 2/3 for the sinusoidal case.

COMPUTER ANALYSIS

To compare the accuracy of the square law theory with that of the bulk–charge theory a simple program was written where the following instructions were performed:

1. Read from an input file V_{gmax}, X0, NA, Z/L and μ'_n where V_{gmax} is the maximum value of the gate voltage, X0 is the thickness of the oxide layer, NA is the doping concentration of the p-type semiconductor, Z/L is the ratio of the width to the length of the channel and μ'_n is the effective mobility in the channel.

2. Using Eq. 13 find V_{dsat}; the drain voltage at pinchoff when the gate voltage V_g is equal to V_{gmax}. The equations and definitions for the functions appearing in Eq. 13 are given in [3].

$$V_{dsat} = V_g - V_T - V_W\{\, [(V_g - V_T)/2\phi_F + (1+ V_W/4\phi_F)^2\,]^{1/2} - (1+ V_W/4\phi_F)\} \quad (13)$$

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3. Using Eq. 14 find I_{dss} by setting the gate voltage V_g equal to V_{gmax} [4].

$$I_{dsat} = (Z/L)(\mu'_n)C_0\{(V_g - V_T)V_{dsat} - V_{dsat}^2/2 - 4V_W\phi_F/3[(1+ V_{dsat}/2\phi_F)^{3/2} - (1+ 3V_{dsat}/4\phi_F)]\} \quad (14)$$

4. Define 1,440 points by incrementing theta from 0 to 360 degrees in increments of 360/1440 degrees.

5. At each of these points calculate V_g given by Eq. 2 and using these values of V_g, calculate I_{dsat} at these 1440 points using Eq. 14.

6. Calculate I_{dsat}/I_{dss} at these 1440 points and plot I_{dsat}/I_{dss} in Figure 1.

7. Calculate the Fourier Coefficients I_0 and I_1, using Simpsons rule.

8. Calculate EFF0 = $I_1/2I_0$.

The results are shown for twelve cases in Table 1. The values of EFF0 in Table 1 are within 0.5% of the value calculated using Eq. 12. Figure 1 shows plots of I_{ds}/I_{dss} as a function of THETA for all twelve cases. I_{dsat}/I_{dss} calculated using Eq. 5 is also plotted in Figure 1. The curves are so close to one another that they appear as a thickened curve. Thus, the square law theory is in very good agreement with the bulk-charge theory for the calculation of I_{dsat}/I_{dss}. The two theories differ, however, in the values of I_{dss} and V_{dsat} [5].

CASE	VGMAX	X0	IDSS	VT	I0	I1	EFF0
1	3	0.5E-05 0.1E+16	0.842E-04	0.798	0.3733	0.499	0.669
2	3	0.1E-04 0.1E+16	0.311E-04	0.998	0.3721	0.499	0.670
3	3	0.5E-05 0.1E+17	0.352E-04	1.410	0.3720	0.499	0.670
4	3	0.1E-04 0.1E+17	0.418E-05	2.103	0.3724	0.499	0.670
5	7	0.5E-05 0.1E+16	0.685E-03	0.798	0.3729	0.499	0.669
6	7	0.1E-04 0.1E+16	0.294E-03	0.998	0.3712	0.499	0.672
7	7	0.5E-05 0.1E+17	0.467E-03	1.410	0.3701	0.498	0.673
8	7	0.1E-04 0.1E+17	0.140E-03	2.103	0.3677	0.497	0.676
9	12	0.5E-05 0.1E+16	0.227E-02	0.798	0.3729	0.499	0.669
10	12	0.1E-04 0.1E+16	0.102E-02	0.998	0.3711	0.499	0.672
11	12	0.5E-05 0.1E+17	0.175E-02	1.410	0.3697	0.498	0.674
12	12	0.1E-04 0.1E+17	0.619E-03	2.103	0.3662	0.497	0.678

Table 1.

For a given value of R_L increasing V_0 does not increase the output power since the drain current is saturated. It will however increase the DC power and hence reduce the efficiency. Decreasing V_0 on the other hand will decrease the output power since for part of the cycle the drain current will be less than the saturation current. For a given value of R_L, Eqs. 9, 10 and 12 give the maximum power and the efficiency at the maximum power. The power and efficiency will be increased by increasing R_L and therefore, the load resistance should be as large as possible without exceeding the maximum allowed drain voltage.

The MOSFET: The Half Sinusoidal Input Voltage Excitation

The second case to be considered is the half sinusoidal case, where for half of the cycle V_g is a sinusoid with a maximum value of V_{gmax} and a minimum of V_T and for the other half of the cycle, V_g is equal to V_T. V_g is given by Eq. 15

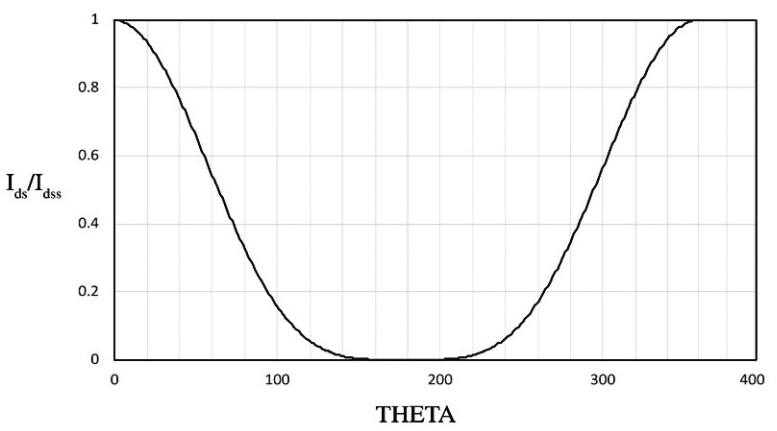

Figure 1: I_{dsat}/I_{dss} as a function of THETA computed using Eq. 5 and twelve cases analyzed by computer program (shown in Table 1)

$$V_g = V_T + (V_{gmax} - V_T)\cos(\omega t) \qquad -90° < \omega t < 90°$$

$$V_g = V_T \qquad \text{otherwise} \quad (15)$$

Substituting V_g into Eq.1 and dividing by Eq. 4 yields

$$I_{dsat}/I_{dss} = \cos^2(\omega t) \qquad -90° < \omega t < 90°$$

$$I_{dsat}/I_{dss} = 0 \qquad \text{otherwise} \quad (16)$$

I_{dsat}/I_{dss} is then equal to the product of $\cos^2(\omega t)$ and a square wave of unit magnitude centered at $\omega t=0$. Using the Fourier expansion of the square wave and the trigonometric identity for $\cos^2(\omega t)$, I_{dsat}/I_{dss} can be written as:

$$I_{dsat}/I_{dss} = .5(1+\cos(2\omega t))(.5 + (2/\pi)(\cos(\omega t) - \cos(3\omega t)/3 + \cos(5\omega t)/5...) \quad (17)$$

Multiplying the two factors and using the trigonometric identity for the product of two cosines yields Eq. 18.

$$I_{dsat}/I_{dss} = .25 + (4/3\pi)\cos(\omega t) + (.25)\cos(2\omega t) + (4/17\pi)\cos(3\omega t) + \ldots \quad (18)$$

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It can be seen from Eq. 18 that I_1 is equal to $4/3\pi$ and I_0 is equal to .25. The DC power is given by Eq. 19;

$$P_0 = I_0 I_{dss} V_0 = I_{dss} V_0/4 . \quad (19)$$

The drain current is not a function of the drain voltage when the MOSFET is in saturation; it is only a function of the gate voltage and it therefore is not affected by the load impedance. Since only the fundamental frequency is desired at the output, the load impedance should present a short-circuit at all of the harmonic frequencies. Only voltage at the fundamental frequency will then appear across the drain and the load resistor. For a given value of V_0 the load resistance R_L is given by Eq. 8. The output power is given by Eq. 10, which for $I_1 = 4/3\pi$ is given by Eq. 20.

$$P_1 = I_{dss} (4/3\pi) (V_0 - (V_{gmax} - V_T)/2 = I_{dss}(.212) (V_0 - (V_{gmax} - V_T)) \quad (20)$$

The efficiency equal to P_1/P_0 where $I_1 = 4/3\pi$ and $I_0 = .25$ is given by Eq. 21.

$$Eff = EFF0(V_0 - (V_{gmax} - V_T)/V_0 = (.849)(V_0 - (V_{gmax} - V_T))/V_0 \quad (21)$$

Comparison of Eqs. 20 and 21 with Eqs. 11 and 12 shows that the half sine wave input excitation will give greater efficiency than the sine wave excitation, but less output power.

The MOSFET: Square Wave Input Voltage Excitation

The third case to be considered is a square wave excitation, where for half of the cycle V_g is equal to V_{gmax} and for the other half of the cycle V_g is equal to V_T. V_g is given by Eq. 22.

$$V_g = V_{gmax} \quad -90° < \omega t < 90°$$

$$V_g = V_T \quad \text{otherwise} \quad (22)$$

Substituting V_g into Eq. 1 and dividing by Eq. 4 yields:

$$I_{dsat}/I_{dss} = 1 \quad -90° < \omega t < 90°$$

$$I_{dsat}/I_{dss} = 0 \quad \text{otherwise} \quad (23)$$

I_{dsat}/I_{dss} is a square wave of unity magnitude, centered at ωt equal to zero, whose Fourier series is given by Eq. 24.

$$I_{dsat}/I_{dss} = (.5 + (2/\pi)\text{Cos}(\omega t) - (2/3\pi)\text{Cos}(3\omega t) + (2/5\pi)\text{Cos}(5\omega t)) \ \ldots\ldots\ldots) \quad (24)$$

It can be seen from Eq. 24 that I_1 is equal to $2/\pi$ and I_0 is equal to .5.

The drain current is not a function of the drain voltage when the MOSFET is in saturation; it is only a function of the gate voltage and it therefore is not affected by the load impedance. Since only the fundamental frequency is desired at the output, the load impedance should present a short-circuit at all of the harmonic frequencies. Only voltage at the fundamental frequency will then appear across the load resistor. For a given value of V_0 the load resistance R_L is given by Eq. 8. The output power is given by Eq. 10, which for $I_1 = 4/3\pi$ is given by Eq. 25.

$$P_1 = I_{dss} (2/\pi) (V_0 - (V_{gmax} - V_T)/2 = (.318) I_{dss} (V_0 - (V_{gmax} - V_T)) \quad (25)$$

The efficiency equal to P_1/P_0 is given by Eq. 26 for $I_1 = 2/\pi$ and $I_0 = .5$.

$$Eff = [I_1/(2 I_0)][(V_0 - (V_{gmax} - V_T)/V_0] = (.636)(V_0 - (V_{gmax} - V_T))/V_0 \quad (26)$$

Comparison of the values of EFF0 and P^1 for the sine wave, the half sine wave and square wave cases show that the square wave input excitation gives the greatest output power, while the half sine wave input excitation gives the greatest efficiency.

Conclusion

The maximum power and the maximum efficiency at the maximum power have been derived for the MOSFET amplifier when the MOSFET is in saturation over the entire cycle. Three cases were considered: the gate voltage is a sinusoid, a half sinusoid and a square wave. The MOSFET was analyzed using the square law theory. The results were compared to the results using the bulk-charge theory and it was found that the square law theory is in very good agreement with the bulk-charge theory for I_{dsat}/I_{dss}. The two theories differ in the value of I_{dss} and in the value of V_{dsat}. Equations are given for the maximum output power and the efficiency, load resistance and DC voltage and at the maximum output power.

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[4] Ibid page 626.

[5] Ibid page 627

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